

IN THE CLAIMS

Please amend the claims to read as follows:

1-17. (Canceled)

18. (Currently Amended) A nonvolatile semiconductor memory device comprising:
a memory cell array including two pages; and
a control circuit configured to read data stored in one page of the memory cell array and to ~~write the data to~~ rewrite part of the read data and write the rewritten data in the other page of the memory cell array,
wherein a part of the data in one page is different from a corresponding part of the data in the other page of the memory cell array.

19. (Previously Presented) The nonvolatile semiconductor memory device according to claim 18, wherein the memory cell array includes a plurality of memory blocks and each of said plurality of memory blocks includes a plurality of pages.

20. (Previously Presented) The nonvolatile semiconductor memory device according to claim 19, wherein one page of the memory cell array and the other page of the memory cell array are included in different memory blocks.

21. (Previously Presented) The nonvolatile semiconductor memory device according to claim 18, wherein the control circuit includes a sense/latch circuit that senses and latches the data stored in one page of the memory cell array.

22. (Previously Presented) The nonvolatile semiconductor memory device according to claim 21, wherein the sense/latch circuit includes a plurality of latch circuits.

23. (Previously Presented) The nonvolatile semiconductor memory device according to claim 22, wherein said plurality of latch circuits are specified according to their addresses, and writing of the data is performed by the specified latch circuit.

24. (Previously Presented) The nonvolatile semiconductor memory device according to claim 23, wherein the control circuit includes a latch specifying circuit which specifies said plurality of latch circuits by the address.

25. (Previously Presented) The nonvolatile semiconductor memory device according to claim 24, wherein the latch specifying circuit is a column decoder circuit.

26. (Previously Presented) The nonvolatile semiconductor memory device according to claim 18, wherein the control circuit includes a page specifying circuit which specifies the page in the memory cell array.

27. (Previously Presented) The nonvolatile semiconductor memory device according to claim 25, wherein the page specifying circuit is a row decoder circuit.

28. (Previously Presented) The nonvolatile semiconductor memory device according to claim 21, wherein the control circuit includes a data I/O circuit connected to the sense/latch circuit which outputs data latched by the sense/latch circuit and which gives supplied data to be written to the sense/latch circuit.

29. (Previously Presented) The nonvolatile semiconductor memory device according to claim 18, wherein the memory cell array comprises a plurality of non-volatile transistors, said plurality of non-volatile transistors are serially connected to form a NAND cell.